REMARKS

Claims 1-50 are pending in this application. Claims 36-50 were withdrawn from consideration by the Examiner.

In response to the election requirement, Applicants hereby elect "the first embodiment represented by Figs. 1-36" without traverse. Applicants believe that at least claims 1-35 correspond to Figs. 1-36. Furthermore, upon the allowance of the generic claim, Applicants are entitled to consideration of claims to additional species.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**".

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the undersigned Deposit Account, Account No. 01-2135 (reference 501.39484X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph [0112] on page 18 of the substitute specification has been amended as follows:

[0112] With respect to the dry etching technology for forming the isolation trenches 2a, when an etching with large anisotropy is utilized in order to increase the integrity of the isolation trenches 2a, the radius of curvature of the bottom corner within the trenches becomes small, so that stress concentrates on the corner parts ~~And~~ and transposition occurs within the semiconductor substrate 1 so as to degrade the element isolation characteristics.

Paragraph [0130] beginning on page 27 of the substitute specification has been amended as follows:

[0130] Then, a gate oxidization treatment is applied to the semiconductor substrate 1, and, thereby, as shown in Fig. 9, a gate insulating film 8a made of silicon oxide, or the like, having, for example, a thickness of approximately 4nm, is formed on the surface of the semiconductor substrate 1 which is exposed from the trenches 7b. After that, a gate insulating film 8b made of silicon nitride, or the like, having, for example, a thickness of approximately 10nm, is deposited thereon (within the trenches 7a and 7b) through a low pressure CVD method, or the like. Thereby, a gate insulating film 8 (8a, 8b) is formed within the trenches 7a and 7b. In the present Embodiment 1, the deterioration of the coverage of the gate insulating film 8a within the trenches 7a and 7b can be compensated for by forming a gate insulating film 8b

through a CVD method, or the like, and, therefore, it becomes possible to increase the withstanding voltage of the gate insulation. Fig. 10 schematically shows the case where the gate insulating film is formed only through a thermal oxidization method. In this case, the ~~covdrage~~ coverage of the gate insulating film 8a deteriorates due to the occurrence of stress accompanying the formation of the thermal oxide film in the regions E of the bottom corners within the trenches 7b, so that an electric field concentration easily occurs at those locations. That is to say, a gate insulation breakdown occurs at these places so that a leakage current flows between the gate electrodes G and the semiconductor substrate 1. Since an uneven part can easily be created on the interface part between the trenches 7a and 7b, this phenomenon easily occurs in the case where the gate insulating film is formed only through the thermal oxidization method. Here, the symbols SD denote source and drain regions. On the other hand, Figs. 11 (a) and 11 (b) schematically show the case where the gate insulating film is formed through a CVD method. Fig. 11 (b) is an enlarged view of the region E of Fig. 11 (a). In this case, the gate insulating film grows in a conformal manner with respect to the base, and, therefore, the coverage in the bottom corners within the trenches can be increased so that the problem of the deterioration of the withstanding voltage of the insulation of the bottom corners can be controlled or prevented. In addition, in the case where the gate insulating film is formed of a layered film through a thermal oxidization method and a CVD method, the gate insulating film 8b formed through the CVD method can compensate for the locations which cannot be covered with the gate insulating film 8a formed through the thermal oxidization method, and, therefore, it becomes possible to control or prevent the above described problem.

Paragraph [0134] beginning on pag 30 of th substitute specification has been amended as follows:

[0134] Next, as shown in Fig. 17, the gate electrode forming film 9a is, again, etched back through an isotropic dry etching treatment. At this time, the insulating film 5 on the semiconductor substrate 1 and the ~~insulati-ng~~ insulating film 10, which is filled in the voids of ~~date~~ gate electrode forming film 9a, are used as an etching mask. The reason why the insulating film 10 is formed in the voids in this way is that, if the insulating film 10 does not exist, the etching proceeds more in the void parts than in other parts at the time of the etching back treatment of the gate electrode forming film 9a, and, therefore, the gate insulating film 8b is exposed so as to include the risk of defects. Accordingly, in case such a problem doesn't occur, the step of formation of the insulating film 10 may be eliminated. Then, an oxidization process is applied to the semiconductor substrate 1 and, thereby, amorphous silicon is oxidized, and, after that, the part oxidized by this is removed by hydrofluoric acid, or the like. Thereby, it becomes possible to remove the residue of amorphous silicon even if it remains within the trenches 7a and 7b. After that, as shown in Fig. 18, a conductive film 11 made of, for example, titanium (Ti), or the like, is deposited through a CVD method, a spattering method, or the like, and then the conductive film 11 and the gate electrode forming film 9a cause a silicidation reaction through the process of annealing. After that, by removing the conductive film 11, which hasn't reacted, using hydrogen peroxide, or the like, word lines WL (gate electrodes 9) made of, for example, titanium silicide, or the like, are formed within the trenches 7a and 7b, as shown in Figs. 19 and 20. In the present Embodiment 1, microscopic

trenches 7a and 7b are filled in with amorphous silicon which makes an effective filling in possible, and, after that, the amorphous silicon is made to be silicide through silicidation, and, thereby, the gate electrodes 9 made of titanium silicide, or the like, which is of low resistance, can be formed within the trenches 7a and 7b in an effective filled in manner. Here, the filled in gate electrode material is not limited to titanium silicide, but, rather, can be changed in a variety of ways. For example, the surface of the titanium silicide can be further nitrided so as to gain a structure where titanium nitride is layered. In this case, it becomes possible to increase the withstanding characteristics of the gate electrode at the time of the cleaning treatment after contact holes are created in the insulating film so that gate electrodes are exposed in the later steps. In addition, by using metal, such as tungsten, the resistance of the word lines WL can be reduced to a great extent. Furthermore, a structure can be gained wherein, for example, a polycrystal silicon of low resistance, tungsten nitride and tungsten are stacked in this order from the lower layer. In this case, by making the lowest layer of polycrystal silicon p-type, the threshold voltage can be made larger by the difference of work function with the n-type silicon, and, therefore, it becomes possible to secure a desired threshold voltage under the condition where the impurity concentration of the semiconductor substrate 1 is made lower. This effect can be gained in the case where tungsten is used as a gate electrode material. In addition, the gate electrodes.may be constructed of, only, a polycrystal silicon of low resistance.

Paragraph [0154] beginning on page 46 of the substitute specification has been amended as f llows:

[0154] Next, after depositing an insulating film made of silicon nitride of, for example, the thickness of approximately 20nm, on the semiconductor substrate 1 through a CVD method, or the like, this is etched back through a dry etching method so as to form, as shown in Fig. 39, side walls 41 on the upper parts (side surfaces between the top surfaces of the gate electrodes 9 and the aperture parts of the trenches 7) of the inner surfaces of the trenches 7. Those side walls 41 are for controlling or preventing the peeling of the gate insulating film 8a. Then, as shown in Fig. 40, after depositing an insulating film 42 made of silicon nitride of, for example, approximately 150nm ~~on.the~~ on the main surface of the semiconductor substrate 1 through a CVD method, or the like, by polishing and reducing this by, for example, approximately 80nm through a CMP method, or the like, the top surface of the insulating film 42 is made flat. Then, the parts of this insulating film 42 which are deposited on the peripheral circuit region, as described in the above Embodiment 1, are removed through a photolithographic technology and a dry etching technology. Accordingly, the insulating film 42 is formed on the main surface of the semiconductor substrate 1 so as to cover the memory cell region. In addition, part of the insulating film 42 is filled in the upper parts within the trenches 7 so as to have the same functions as a cap insulating film.

Paragraph [0157] on page 48 of the substitute specification has been amended as follows:

[0157] That is to say, at the time of formation of contact holes 21 in the insulating film 42 through a dry etching method, or the like, by carrying out the etching under a condition where the etching rate of silicon nitride is faster than that

for silicon oxide, it becomes possible to control or prevent the upper parts of the isolation parts 2 from being shaved through the etching even in the case where over-etching takes place under a condition where, for example, the isolation parts 2 are exposed from the bottoms of the contact holes 21. Accordingly, it becomes possible to increase~~,~~ the reliability and yield of the MIS·FETs for memory cell selection.

Paragraph [0112] on page 18 of the substitute specification has been amended as follows:

[0112] With respect to the dry etching technology for forming the isolation trenches 2a, when an etching with large anisotropy is utilized in order to increase the integrity of the isolation trenches 2a, the radius of curvature of the bottom corner within the trenches becomes small, so that stress concentrates on the corner parts ~~And~~ and transposition occurs within the semiconductor substrate 1 so as to degrade the element isolation characteristics.

Paragraph [0130] beginning on page 27 of the substitute specification has been amended as follows:

[0130] Then, a gate oxidization treatment is applied to the semiconductor substrate 1, and, thereby, as shown in Fig. 9, a gate insulating film 8a made of silicon oxide, or the like, having, for example, a thickness of approximately 4nm, is formed on the surface of the semiconductor substrate 1 which is exposed from the trenches 7b. After that, a gate insulating film 8b made of silicon nitride, or the like, having, for example, a thickness of approximately 10nm, is deposited thereon (within

the trenches 7a and 7b) through a low pressure CVD method, or the like. Thereby, a gate insulating film 8 (8a, 8b) is formed within the trenches 7a and 7b. In the present Embodiment 1, the deterioration of the coverage of the gate insulating film 8a within the trenches 7a and 7b can be compensated for by forming a gate insulating film 8b through a CVD method, or the like, and, therefore, it becomes possible to increase the withstanding voltage of the gate insulation. Fig. 10 schematically shows the case where the gate insulating film is formed only through a thermal oxidization method. In this case, the ~~covdrage~~ coverage of the gate insulating film 8a deteriorates due to the occurrence of stress accompanying the formation of the thermal oxide film in the regions E of the bottom corners within the trenches 7b, so that an electric field concentration easily occurs at those locations. That is to say, a gate insulation breakdown occurs at these places so that a leakage current flows between the gate electrodes G and the semiconductor substrate 1. Since an uneven part can easily be created on the interface part between the trenches 7a and 7b, this phenomenon easily occurs in the case where the gate insulating film is formed only through the thermal oxidization method. Here, the symbols SD denote source and drain regions. On the other hand, Figs. 11 (a) and 11 (b) schematically show the case where the gate insulating film is formed through a CVD method. Fig. 11 (b) is an enlarged view of the region E of Fig. 11 (a). In this case, the gate insulating film grows in a conformal manner with respect to the base, and, therefore, the coverage in the bottom corners within the trenches can be increased so that the problem of the deterioration of the withstanding voltage of the insulation of the bottom corners can be controlled or prevented. In addition, in the case where the gate insulating film is formed of a layered film through a thermal oxidization method and a CVD method,

the gate insulating film 8b formed through the CVD method can compensate for the locations which cannot be covered with the gate insulating film 8a formed through the thermal oxidization method, and, therefore, it becomes possible to control or prevent the above described problem.

Paragraph [0134] beginning on page 30 of the substitute specification has been amended as follows:

[0134] Next, as shown in Fig. 17, the gate electrode forming film 9a is, again, etched back through an isotropic dry etching treatment. At this time, the insulating film 5 on the semiconductor substrate 1 and the ~~insulati ng~~ insulating film 10, which is filled in the voids of ~~date~~ gate electrode forming film 9a, are used as an etching mask. The reason why the insulating film 10 is formed in the voids in this way is that, if the insulating film 10 does not exist, the etching proceeds more in the void parts than in other parts at the time of the etching back treatment of the gate electrode forming film 9a, and, therefore, the gate insulating film 8b is exposed so as to include the risk of defects. Accordingly, in case such a problem doesn't occur, the step of formation of the insulating film 10 may be eliminated. Then, an oxidization process is applied to the semiconductor substrate 1 and, thereby, amorphous silicon is oxidized, and, after that, the part oxidized by this is removed by hydrofluoric acid, or the like. Thereby, it becomes possible to remove the residue of amorphous silicon even if it remains within the trenches 7a and 7b. After that, as shown in Fig. 18, a conductive film 11 made of, for example, titanium (Ti), or the like, is deposited through a CVD method, a spattering method, or the like, and then the conductive film 11 and the gate electrode forming film 9a cause a silicidation reaction through the

process of annealing. After that, by removing the conductive film 11, which hasn't reacted, using hydrogen peroxide, or the like, word lines WL (gate electrodes 9) made of, for example, titanium silicide, or the like, are formed within the trenches 7a and 7b, as shown in Figs. 19 and 20. In the present Embodiment 1, microscopic trenches 7a and 7b are filled in with amorphous silicon which makes an effective filling in possible, and, after that, the amorphous silicon is made to be silicide through silicidation, and, thereby, the gate electrodes 9 made of titanium silicide, or the like, which is of low resistance, can be formed within the trenches 7a and 7b in an effective filled in manner. Here, the filled in gate electrode material is not limited to titanium silicide, but, rather, can be changed in a variety of ways. For example, the surface of the titanium silicide can be further nitrided so as to gain a structure where titanium nitride is layered. In this case, it becomes possible to increase the withstanding characteristics of the gate electrode at the time of the cleaning treatment after contact holes are created in the insulating film so that gate electrodes are exposed in the later steps. In addition, by using metal, such as tungsten, the resistance of the word lines WL can be reduced to a great extent. Furthermore, a structure can be gained wherein, for example, a polycrystal silicon of low resistance, tungsten nitride and tungsten are stacked in this order from the lower layer. In this case, by making the lowest layer of polycrystal silicon p-type, the threshold voltage can be made larger by the difference of work function with the n-type silicon, and, therefore, it becomes possible to secure a desired threshold voltage under the condition where the impurity concentration of the semiconductor substrate 1 is made lower. This effect can be gained in the case where tungsten is used as a gate

electrode material. In addition, the gate electrodes.may be constructed of, only, a polycrystal silicon of low resistance.

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[0154] Next, after depositing an insulating film made of silicon nitride of, for example, the thickness of approximately 20nm, on the semiconductor substrate 1 through a CVD method, or the like, this is etched back through a dry etching method so as to form, as shown in Fig. 39, side walls 41 on the upper parts (side surfaces between the top surfaces of the gate electrodes 9 and the aperture parts of the trenches 7) of the inner surfaces of the trenches 7. Those side walls 41 are for controlling or preventing the peeling of the gate insulating film 8a. Then, as shown in Fig. 40, after depositing an insulating film 42 made of silicon nitride of, for example, approximately 150nm ~~on the~~ on the main surface of the semiconductor substrate 1 through a CVD method, or the like, by polishing and reducing this by, for example, approximately 80nm through a CMP method, or the like, the top surface of the insulating film 42 is made flat. Then, the parts of this insulating film 42 which are deposited on the peripheral circuit region, as described in the above Embodiment 1, are removed through a photolithographic technology and a dry etching technology. Accordingly, the insulating film 42 is formed on the main surface of the semiconductor substrate 1 so as to cover the memory cell region. In addition, part of the insulating film 42 is filled in the upper parts within the trenches 7 so as to have the same functions as a cap insulating film.

Paragraph [0157] on pag 48 of the substitute specification has been amended as foll ws:

[0157] That is to say, at the time of formation of contact holes 21 in the insulating film 42 through a dry etching method, or the like, by carrying out the etching under a condition where the etching rate of silicon nitride is faster than that for silicon oxide, it becomes possible to control or prevent the upper parts of the isolation parts 2 from being shaved through the etching even in the case where over-etching takes place under a condition where, for example, the isolation parts 2 are exposed from the bottoms of the contact holes 21. Accordingly, it becomes possible to increase~~,~~ the reliability and yield of the MIS·FETs for memory cell selection.